Amendments to the Claims

Please amend claims 1, 4, 8, 9, 13, 14 and 15. The Claim Listing below will replace all prior versions of the claims in the application. No new matter has been added by way of these amendments.

Claim Listing

1. (Currently amended) A method of reducing data path latency in digitally processing a sequence of data samples, the data path latency being associated with a transient processing operation on the data samples, comprising:

during the transient processing operation on the data samples reading the sequence of data samples into a tapped clocked delay chain;

during the transient processing operation on the data samples, processing data samples from taps on the clocked delay chain; and

in response to receiving a signal of completion of ~~a~~ the transient processing ~~event~~ operation on the data samples, shifting data samples rapidly out of the clocked delay chain at a higher output rate than an input rate of data samples coming into the clocked delay chain; and

dynamically reducing the length of the clocked delay chain as data samples continue to be read into the clocked delay chain.

2. (Previously Presented) The method of Claim 1 wherein the data samples are from a data packet.

3. (Previously Presented) The method of Claim 2 wherein the data packet conforms to a transmission system selected from the group of 802.11a, 802.11g and HIPERLAN/2 transmission systems.

4. (Currently Amended) The method of Claim 3 wherein the transient processing operation includes a synchronization of the data packet.

5. (Previously Presented) The method of Claim 4 wherein the clocked delay chain comprises a plurality of pipelined registers.

6. (Previously Presented) The method of Claim 5 wherein the reducing the length of the clocked delay chain is performed until a desired length of the clocked delay chain is achieved.

7. (Previously Presented) The method of Claim 5 wherein reducing the length of the clocked delay chain further includes bypassing empty registers.

8. (Currently Amended) A method of reducing data path latency in digitally processing a sequence of data samples of a data packet, the data path latency being associated with synchronization of the data packet, comprising:

upon reception of the data packet, reading the sequence of data samples from the ~~a~~ data packet into a tapped clocked delay chain comprising a plurality of pipelined registers;

processing data samples from taps on the clocked delay chain to synchronize the ~~a~~ data packet;

in response to receiving a signal of completion of synchronization of the data packet, shifting samples rapidly out of the clocked delay chain at a higher output rate than an input rate of data samples coming into the clocked delay chain;

reducing the length of the clocked delay chain by bypassing empty registers as data samples continue to be read into the clocked delay chain; and

repeating the steps of shifting data samples rapidly out of the clocked delay chain at a higher output rate than the input rate and reducing the length of the clocked delay chain.

9. (Currently amended) An apparatus comprising:

a pipeline of registers that store data samples;

logic circuitry which controls each individual register of the pipeline of registers;

a multiplexer having inputs from select registers from the pipeline of registers, and an output; and

a processor which controls the data shifting rates, the logic circuitry, and the output of the multiplexer based on ~~a plurality~~ completion states of a transient processing operation on the data samples ~~events of the apparatus~~.

10. (Original) An apparatus of Claim 9 wherein the data samples are from a data packet.

11. (Previously Presented) The apparatus of Claim 10 data packet conforms to 802.11a, 802.11g and HIPERLAN/2 transmission systems standards.

12. (Original) An apparatus of Claim 11 further comprising a timing recovery module for synchronization of the data packet that initiates a transition in the processor.

13. (Currently amended) An apparatus comprising:

a pipeline of registers that stores data samples of a data packet;

a timing recovery module for synchronization of the data packet that initiates a transition;

logic circuitry which controls each individual register of the pipeline of registers;

a multiplexer having inputs from select registers from the pipeline of registers, and an output; and

a processor having inputs from a timing recovery module for packet synchronization which controls the data shifting rates, the logic circuitry, and the output of the multiplexer based on ~~a plurality~~ completion states of the synchronization of the data packet ~~processing events of the apparatus~~.

14. (Currently amended) An apparatus comprising:

means for reading data samples into a tapped clocked delay chain;

means for processing data samples from taps on the clocked delay chain;

means for shifting data samples out of the clocked delay chain at a higher output rate than an input rate of data samples coming into the clocked delay chain; and

means for dynamically reducing the length of the clocked delay chain in response to receiving a signal of completion of a transient processing operation on the data samples ~~event~~.

15. (Currently amended) Within a digital processor, a method of reducing data path latency in digitally processing data samples comprising:

providing a clocked delay chain with an output rate higher than an input rate;

shifting data samples out of the clocked delay chain at the higher output rate while reading additional data samples into the input end of the clocked delay chain at the input rate in response to receiving a signal of completion of a transient processing operation on the data samples; and

dynamically reducing the length of the delay chain as data samples continue to be read into the clocked delay chain.

16. (Previously Presented) The method of Claim 15 further comprising bypassing an empty portion of clocked delay chain.

17. (Previously Presented) The method of claim 15 performed in response to receiving a signal of completion of a processing event.

18. (Previously Presented) The method of claim 17 wherein the data samples are from a data packet and the signal of completion of a processing event is a sync signal indicating synchronization of the data packet.

19. (Previously Presented) The apparatus of Claim 9 wherein the processor is a state-machine.

20. (Previously Presented) The apparatus of Claim 13 wherein the processor is a state-machine.